



Voice Playback SoC

IPJ5022

Chip Datasheet

Version V1.1

Date 2026-10-12

1 Overview and Block Diagram

IPJ5022 targets voice prompts, audio playback and sound toys. This manual covers SOP16 pins, internal storage, electrical specifications and package requirements. It also provides connections for the supplied audio playback firmware to support schematic and PCB design.

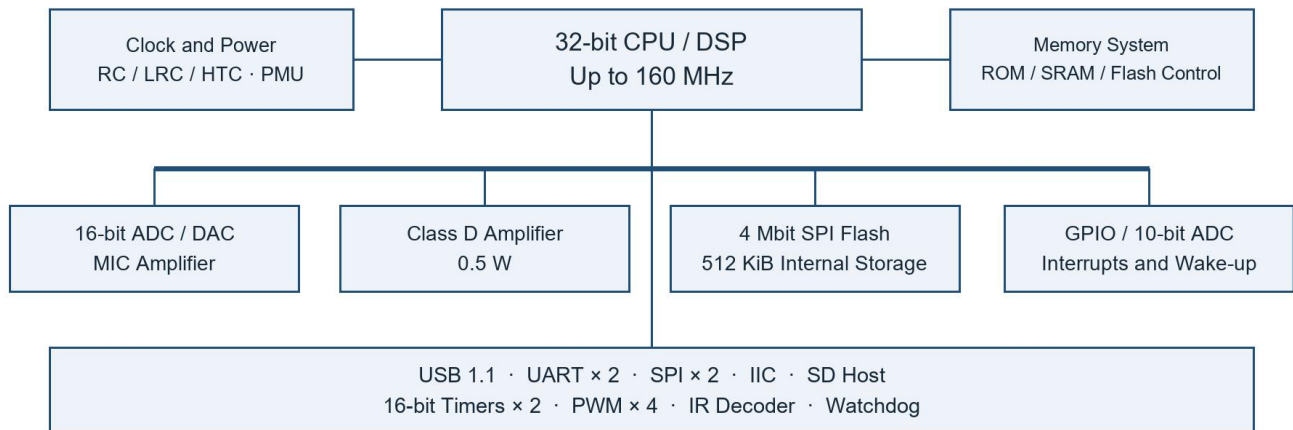
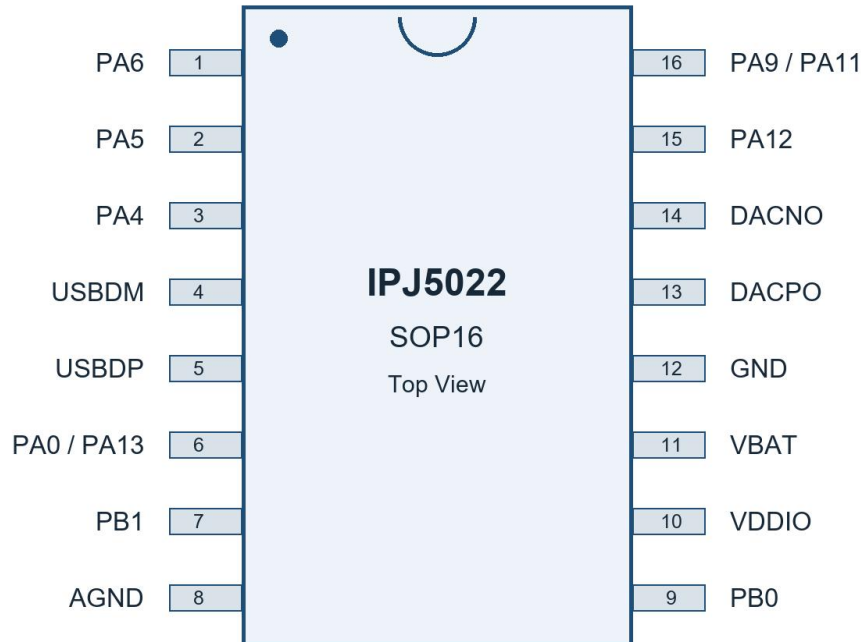


Figure 1-1 Chip functional block diagram

Resource	Specification
Processor and clocks	32-bit CPU up to 160 MHz; internal RC approx. 16 MHz, LRC approx. 32 kHz, HTC 5 MHz
Internal storage	4 Mbit SPI Flash (512 KiB), shared by firmware, resources and configuration
Audio interfaces	16-bit recording ADC, 16-bit DAC, MIC amplifier, 2 analog audio inputs and 0.5 W Class D amplifier
Digital interfaces	USB 1.1 full-speed PHY × 1; UART × 2 (UART1 supports DMA and flow control); SPI × 2 (DMA, master/slave); IIC × 1; SD Host × 1
Timing and control	Two 16-bit timers, 4 PWM channels, infrared remote decoding, watchdog and 10-bit ADC
GPIO and wake-up	8 programmable digital I/Os; USB DP/DM can serve as GPIO; up to 8 external interrupt or wake-up sources
Power and monitoring	VBAT 2.0–5.5 V; IOVDD 2.0–3.4 V; POR; LVD thresholds 1.8–2.5 V in 0.1 V steps
Temperature and package	Operating temperature –40 to +85 °C; SOP16; 4 Mbit (512 KiB) internal Flash

Note: Peripherals require software configuration and share multiplexed pins; not all functions can be routed out simultaneously. Hardware features such as recording are not necessarily enabled in the supplied playback firmware.

2 Package and Pinout



Dot marks pin 1. Two port names on one pin share a physical pad.

Figure 2-1 SOP16 pinout

Key Connections

Pins	Connection
11 VBAT / 10 VDDIO	VBAT is the supply input; VDDIO supplies the GPIO domain. Decouple as specified in the reference design
8 AGND / 12 GND	Analog and digital ground, respectively; provide low-impedance PCB return paths
4 USBDM / 5 USBDP	USB D- / D+; used for the PC connection in the supplied design
13 DACPO / 14 DACNO	Class D differential outputs; connect to the two speaker terminals
6 PA0/PA13 · 16 PA9/PA11	Two internal ports share one package pin; select functions according to the pin table and firmware configuration

Note: Top view. Pin names describe hardware capabilities; see Chapter 6 for UART, button and BUSY assignments in the supplied firmware.

3 Pin Descriptions

I/O = input/output, O = output, P = power, G = ground. Letters in parentheses identify peripheral routing groups. The table lists the alternate functions of each pin.

Pin	Name	Type	Function and Main Alternate Functions
1	PA6	I/O	GPIO; SPI1DIC, SD0DATD
2	PA5	I/O	GPIO; ADC7, SPI0DAT3, SPI1DOC, SD0CMD, SD0CMD, UART0RXA, I2C_SDA(C), PWM1
3	PA4	I/O	GPIO; ADC6, SPI0DAT2, SPI1CLKC, SD0CLKC, SD0CLKD, UART0TXA, I2C_SCL(C), TMR2, PWM0
4	USBDM	I/O	USB D-, default pull-down; ADC5, SPI1DOA, SD0DATC, UART1TXA, I2C_SDA(A)
5	USBDP	I/O	USB D+, default pull-down; ADC4, SPI1CLKA, UART1RXA, I2C_SCL(A)
6	PA0	I/O	GPIO, default pull-up; long-press reset, ADC0, UART0TXB
6	PA13	I/O	GPIO; ADC10, AUX0, MIC_BIAS, CAP0
7	PB1	I/O	GPIO; MIC_IN
8	AGND	G	Analog ground
9	PB0	I/O	GPIO; analog DAC output, ADC13, LVD
10	VDDIO	P	GPIO supply
11	VBAT	P	Battery supply input
12	GND	G	Digital ground
13	DACPO	O	Class D amplifier positive output
14	DACNO	O	Class D amplifier negative output
15	PA12	I/O	GPIO; SPI1DOB, MCAP3
16	PA11	I/O	GPIO; ADC9, SPI1CLKB, MCAP2
16	PA9	I/O	High-voltage GPIO; UART1TXB, UART1RXB, I2C_SDA(D), CAP1, PWM3

Note 1: Pins 6 and 16 each have two internal port names sharing one physical pad. They are not independent external pins and must not be configured as conflicting outputs.

Note 2: PA9 is a high-voltage port, but a separate voltage rating is not specified. Do not assume that it accepts a direct 5 V input.

Note 3: Peripherals such as UART support input/output channel routing. Distinguish the firmware connections in Chapter 6 from the fixed alternate-function names in this table.

4 Power and Electrical Characteristics

4.1 Supply Operating Conditions

Parameter	Min.	Typ.	Max.	Unit
VBAT supply input	2.0	3.7	5.5	V
VDDIO output voltage	2.0	3.0	3.4	V
VDDIO output current	—	—	100	mA

VDDIO voltage conditions: VBAT = 3.7 V, 100 mA load. Output current condition: VBAT = 3.7 V.

4.2 Absolute Maximum Ratings and Temperature

Parameter	Min.	Max.	Unit
Operating ambient temperature Tamb	−40	+85	°C
Storage temperature Tstg	−65	+150	°C
VBAT supply voltage	−0.3	5.5	V
3.3 V I/O input voltage	−0.3	3.6	V

Absolute limits are not recommended continuous operating conditions. I/O levels must also meet Chapter 5 requirements.

4.3 Low-Power Modes and Operating Current

Mode	Specified Value	Stated Conditions
Softoff	< 2 μ A	Other conditions not specified
Powerdown	< 30 μ A	Other conditions not specified
Music playback	< 6 mA	HSB = 80 MHz
Recording	< 11 mA	HSB = 80 MHz

These figures do not represent system current or current with a driven speaker load. Actual consumption depends on supply, firmware, peripherals and volume.

4.4 Power Monitoring

The chip integrates power-on reset (POR) and low-voltage detection (LVD). A 3-bit LVD setting selects thresholds from 1.8 to 2.5 V in 0.1 V steps. Firmware determines how detection is enabled and handled.

5 I/O and Audio Characteristics

5.1 I/O Logic Levels

Parameter	Min.	Typ.	Max.	Unit
Low-level input VIL	-0.3	—	$0.3 \times VDDIO$	V
High-level input VIH	$0.7 \times VDDIO$	—	$VDDIO + 0.3$	V
Low-level output VOL	—	—	0.33	V
High-level output VOH	2.7	—	—	V

Test condition: VDDIO = 3.3 V. Output load current is not specified.

5.2 Drive Strength and Internal Resistors

Port	Normal drive	High drive	Pull-up	Pull-down
PA0, PA4–PA6, PA11–PA13, PB0, PB1	8 mA	64 mA	10 kΩ	60 kΩ
PA9	8 mA	—	10 kΩ	60 kΩ
USBDP	10 mA	—	1.5 kΩ	15 kΩ
USBDM	10 mA	—	180 kΩ	15 kΩ

Pull-up/down tolerance: $\pm 20\%$. PA0 defaults to pull-up; USB DP/DM default to pull-down. Drive ratings do not imply that all pins can continuously source or sink the stated current simultaneously.

5.3 Audio Converters

Block	Parameter	Value	Unit
PB0 DAC	Frequency response	20–16000	Hz
PB0 DAC	THD+N / SNR	-65 / 95	dB
PB0 DAC	Output swing	0.54	V _{rms}
PB0 DAC	Dynamic range	92	dB
PB0 DAC	Output resistance	8.3	kΩ
Recording ADC	Dynamic range / SNR / THD+N	75 / 79 / -70	dB

DAC: Values are typical except the frequency range. Frequency, THD+N, SNR and swing conditions: 1 kHz / 0 dB, 100 kΩ load, A-weighting. Dynamic range uses a -60 dB signal with the same load and weighting. Output resistance conditions are unspecified.

ADC: Typical values; 1 kHz / 210 mV_{rms}, line mode at 6 dB with capacitor, PGAIS = 2.

Class D power is specified as 0.5 W; corresponding supply, load and distortion conditions are not specified. PB0 DAC figures do not characterize the Class D speaker outputs.

6 Firmware Connections and Control

This chapter applies to the current IPJ5022 audio playback firmware. These pin assignments and commands are firmware functions; a blank chip does not provide this behavior automatically.



Figure 6-1 Connections for the audio playback firmware

Signal	Chip Pins	Firmware Behavior
UART TX / RX	PA11 (16)/ PA12 (15)	9600 bps, 8 data bits, no parity, 1 stop bit; cross-connect to the host controller
BUSY	PA0 (6)	High when idle; low during playback; returns high on stop, end of playback or playback failure
Playback button	PB1 (7)	Active low; short press for next track, hold about 1 second to stop
Audio output	DACPO (13)/ DACNO (14)	Connect the speaker across both differential outputs; do not ground either output

UART Data Frames

Request, 6 bytes: AA 55 CMD VL VH EF

Response, 7 bytes: AA 55 (CMD | 80) STATUS VL VH EF

Bytes are hexadecimal. Values are little-endian: VL = low byte, VH = high byte. EF is fixed; no checksum.

CMD	Function and Value	Request Example (Hex)
01	Play track 1–999, limited by the number of audio files	AA 55 01 01 00 EF
02	Stop playback; request value 0	AA 55 02 00 00 EF
03	Set volume to 0–31; example sets volume to 20	AA 55 03 14 00 EF
04	Query status; bit 15 indicates playback, bits 0–14 contain the last track number	AA 55 04 00 00 EF
05	Next track, wrapping to track 1 at the end; request value 0	AA 55 05 00 00 EF
06	Query packaged audio file count; request value 0	AA 55 06 00 00 EF

STATUS: 00 success; 01 unknown command; 02 invalid parameter or resources not ready; 03 playback failure. UART volume uses decimal 0–31. Power-up restores the default volume set during download.

Match interface levels to VDDIO. The PC tool configures startup playback, looping and default volume. Reconnect USB or power-cycle after downloading, then test playback.

7 SOP16 Package Dimensions

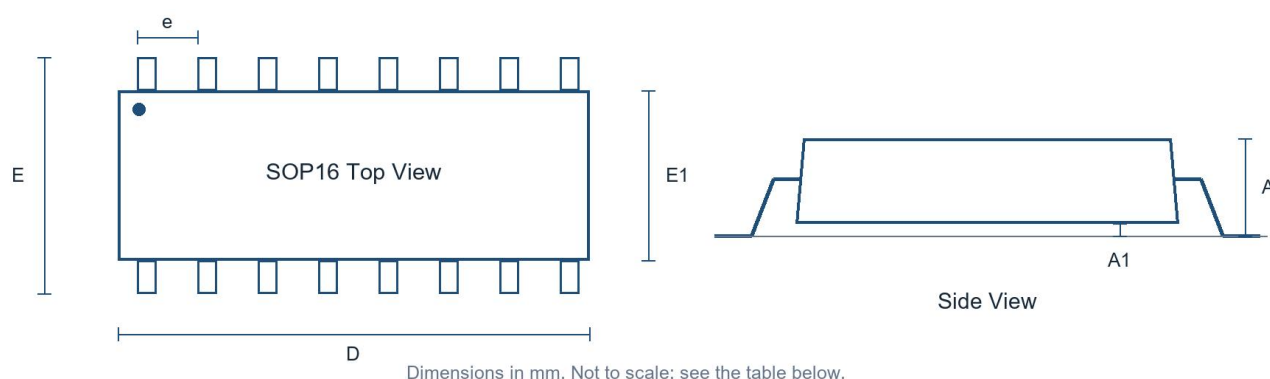


Figure 7-1 SOP16 outline and principal dimensions

Symbol	Description	Min.	Nom.	Max.
A	Overall height	—	—	1.75
A1	Standoff height	0.10	—	0.225
A2	Molded body height	1.30	1.40	1.50
A3	Partial body height	0.60	0.65	0.70
b	Lead width	0.39	—	0.47
b1	Base-metal lead width	0.38	0.41	0.44
c	Lead thickness	0.20	—	0.24
c1	Base-metal lead thickness	0.19	0.20	0.21
D	Body length	9.80	9.90	10.00
E	Overall lead span	5.80	6.00	6.20
E1	Body width	3.80	3.90	4.00
e	Lead pitch	—	1.27 BSC	—
h	Chamfer	0.25	—	0.50
L	Lead foot length	0.50	—	0.80
L1	Reference lead length	—	1.05 REF	—
θ	Lead angle	0°	—	8°

Dimensions are in mm except angles. BSC = basic dimension; REF = reference dimension; “—” = not specified.

Only principal dimensions are labeled. Confirm land patterns, stencil and assembly design against the complete package dimensions and the actual process.

8 Marking and Handling

8.1 Chip Marking and Internal Storage

The internal-storage IPJ5022 variant uses an SOP16 package and includes 4 Mbit (512 KiB) of Flash. The model and storage capacity are listed below.

Product Model	Internal Flash Capacity	Byte Capacity
IPJ5022	4 Mbit	512 KiB

One KiB is 1024 bytes. Available audio space is smaller than total Flash capacity and varies with firmware and resource configuration.

8.2 Moisture Sensitivity and Storage

Item	Requirement	Details
Moisture sensitivity	MSL 3	Handle according to JEDEC J-STD-033
Sealed-bag shelf life	12 months	Storage conditions: < 40 °C and 90% relative humidity
After opening	Within 168 hours	At ≤ 30 °C / 60% RH, or store according to J-STD-033
Peak package temperature	≤ 260 °C	Package-body limit; confirm the complete reflow profile for the assembly process
Moisture exposure	Bake per J-STD-033	For MSL 3: humidity indicator > 10% when checked at 23 ± 5 °C, or opened-bag exposure conditions not met

Define bake temperature, duration and the full reflow profile for the moisture level, package condition and applicable process; do not assume unspecified conditions.

8.3 Design and Assembly Checks

Check orientation and pin 1; confirm VBAT, VDDIO and I/O levels; connect the speaker differentially. Follow the reference design for USB routing, analog return paths and supply decoupling. Verify board current, audio output and temperature rise at the intended load and volume.

9 Revision History and Support

Version	Date	Changes
V1.0	2026-10-11	Initial release: IPJ5022 chip data and firmware interfaces
V1.1	2026-10-12	Standardized product naming and updated the content guide

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Technical Content Guide

The table below points to the relevant chapters in this manual. Firmware interface definitions follow the delivered IPJ5022 firmware and application documentation.

Manual Content	Chapter
Features and block diagram	Chapter 1
SOP16 pins and alternate functions	Chapters 2–3
Power, electrical and audio data	Chapters 4–5
Package dimensions	Chapter 7
Marking, storage and assembly	Chapter 8
UART and PA0 BUSY configuration	Chapter 6; playback firmware 0.1.2; fixed EF trailer

Scope

This manual supports designs using the internal-storage IPJ5022 variant. Confirm unlisted electrical conditions, device differences and manufacturing parameters against the supplied specification and with technical support. Chip capabilities and firmware functions are described separately; software features require configuration and are not all enabled by default.

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